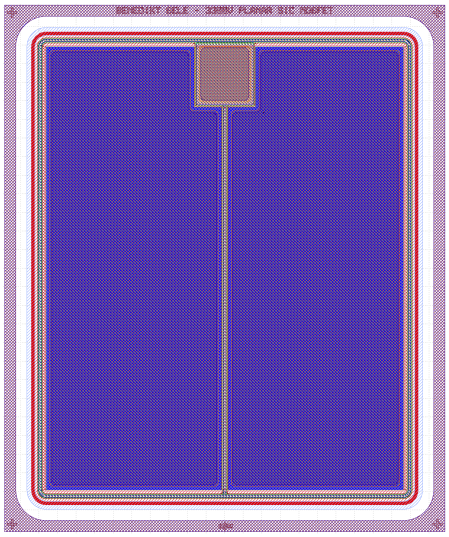
Design of a 3.3 kV SiC MOSFET

Silicon carbide (SiC) MOSFETs are key components for future high-voltage power electronics. Building upon the fabrication process developed during the previous semester, this project completes the digital development of a competitive 3.3 kV planar 4H-SiC MOSFET through TCAD optimisation and lithography mask design.

Sentaurus TCAD cross section showing the optimized net doping profile



KLayout die view showing the complete overlaid lithography mask set

The Challenge

Developing high-voltage SiC MOSFETs requires balancing competing electrical and technological requirements. High breakdown voltage, low specific on-resistance, and a practical threshold voltage must be achieved while ensuring a manufacturable device. This requires the coordinated development of the fabrication process, device geometry, and lithography layout before fabrication can begin.

Device Development

Building upon the previously developed fabrication process, a parameterised TCAD workflow based on Synopsys Sentaurus was established to optimise the active cell and edge termination of a planar 3.3 kV SiC MOSFET. The optimised design was subsequently implemented as a complete lithography mask set, completing the digital workflow from process definition to fabrication.

Result

The project resulted in a competitive planar 3.3 kV 4H-SiC MOSFET with a simulated breakdown voltage exceeding 4.5 kV and a specific on-resistance of approximately 17.4 $m\Omega\,cm^2$. Together with the previously developed fabrication process, the optimised device and lithography mask set constitute a complete fabrication-ready digital design package.

Project at a glance

3.3 kV Planar 4H-SiC MOSFET

- Over 200 individually specified process steps
- TCAD-optimised active cell and edge termination
- Simulated breakdown voltage: >4.5 kV
- Complete lithography mask set
- Die size: 6 mm × 7 mm
- Active area: >500 000 active MOSFET cells
- Complete digital design package

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